What is claimed is:

1. A data processing system comprising:

a set of memory modules for storing program instructions and data, the set of memory modules comprising at least one low-speed memory and at least one high-speed memory, the low-speed and high-speed memories both storing an interrupt vector table individually for recording at least one entry instruction of an interrupt service routine; and

a microprocessor comprising:

a central processing unit (CPU) for executing program instructions and calculating data, wherein the CPU is designed to fetch the program instructions in the low-speed memory when an interruption occurs; and

a memory controller to enable the CPU, under the memory controller's control, to fetch the program instruction and access the data in the set of memory modules, the memory controller also comprising a re-addressing device;

wherein, when the interruption occurs, the CPU generates an interrupt vector address to the memory controller, and if the re-addressing device of the memory controller identifies that the address falls within the address range of the interrupt vector table, the re-addressing device sends out an enable signal to the high-speed memory to enable the CPU to fetch the corresponding entry instruction of the interrupt service routines in the high-speed memory, instead of the predetermined low-speed memory, so as to reduce the interrupt latency when fetching the program instruction.

2. The data processing system of claim 1, wherein the re-addressing device comprises:

a first address decoder for decoding an original address generated by the CPU to identify whether the original address falls within the address range of the interrupt vector table, and to generate a corresponding identifying signal;

a multiplexer for selecting between the original address generated by the CPU and a predetermined re-directing address as a valid address according to the identifying signal; and

a second address decoder for decoding the valid address generated by the multiplexer to determine whether the enable signal is sent to the high-speed memory or the low-speed memory.

3. The data processing system of claim 2, wherein the re-directing address is programmable, and falls within the address range of the high-speed memory, distinguishably from the vector addresses of the low-speed memory.

4. The data processing system of claim 1, wherein the microprocessor further comprises an on-chip high-speed memory, and the on-chip high-speed memory also comprises an interrupt vector table for recording at least one entry instruction of the interrupt service routines, and the vector address range is the same as the vector address range of the interrupt vector table of the low-speed memory.

5. The data processing system of claim 4, wherein the re-addressing device comprises:

a first address decoder for decoding an original address generated by the CPU to determine whether the original address falls within the address range of the interrupt vector table, and to generate a corresponding on-chip enable signal to enable the on-chip high-speed memory;

a second address decoder for decoding the original address generated by the

CPU to determine whether the original address falls within the address range of the high-speed or the low-speed memory, and correspondingly to generate a high-speed enable signal to enable the high-speed memory, or to generate an identifying signal of the low-speed memory; and

an XOR gate for receiving the on-chip enable signal and the identifying signal of the low-speed memory to perform exclusive-or operation, and correspondingly to generate a low-speed enable signal to enable the low-speed memory.

6. The data processing system of claim 1, wherein the low-speed memory is a non-volatile memory.

7. The data processing system of claim 6, wherein the non-volatile memory is an electrical programmable read-only memory (EPROM).

8. The data processing system of claim 6, wherein the non-volatile memory is a flash read-only memory (Flash ROM).

9. The data processing system of claim 1, wherein the high-speed memory is a volatile memory.

10. The data processing system of claim 9, wherein the volatile memory is an external dynamic random access memory (DRAM) built outside the microprocessor.

11. The data processing system of claim 9, wherein the volatile memory is a built-in static random access memory (SRAM) in the microprocessor.

12. The data processing system of claim 1, wherein the microprocessor is a non-PC architecture microprocessor.

13. The data processing system of claim 1, wherein the data processing system

further comprises a power source for providing electrical power to the data processing system, and when the power source is shut down, the program instructions and data stored in the high-speed memory are lost; however the program instructions and data stored in the low-speed memory are preserved.

14. The data processing system of claim 1, wherein the data processing system further comprises a bus connected to the CPU, the memory controller, and the set of memory modules for transmitting the program instructions and data.